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Impact of oxidation and reduction annealing on the electrical properties of $Ge/La_2O_3/ZrO_2$ gate stacks

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ABSTRACT

The paper addresses the passivation of Germanium surfaces by using layered La_2O_3/ZrO_2 high-*k* dielectrics deposited by Atomic Layer Deposition to be applied in Ge-based MOSFET devices. Improved electrical properties of these multilayered gate stacks exposed to oxidizing and reducing ambient during thermal post treatment in presence of thin Pt cap layers are demonstrated. The results suggest the formation of thin intermixed $La_xGe_yO_z$ interfacial layers with thicknesses controllable by oxidation time. This formation is further investigated by XPS, EDX/EELS and TEM analysis. An additional reduction annealing treatment further improves the electrical properties of the gate dielectrics in contact with the Ge substrate. As a result low interface trap densities on (100) Ge down to 3×10^{11} eV^{-1} cm^{-2} are demonstrated. The formation of the high-*k* $La_xGe_yO_z$ layer is in agreement with the oxide densification theory and may explain the improved interface trap densities. The scaling potential of the respective layered gate dielectrics used in Ge-based MOS-based device structures to EOT of 1.2 nm or below is discussed. A trade-off between improved interface trap density and a lowered equivalent oxide thickness is found.

1. Introduction

Germanium (Ge) is a candidate to be integrated as a high mobility channel material in the complementary metal–oxide–semiconductor (CMOS) process flow at or below technology nodes of 16 nm [1,2]. One key reason for an increased scientific interest is the four times increased hole and two times increased electron mobility in bulk Ge compared to Si substrates [1]. Additionally, increased hole and electron mobility are reported in strained Ge substrates [3]. Until recently the lack of a suitable interface passivation methodology has hindered the possible application of Ge substrates in scaled CMOSFET device technologies, relying on the use of scaled high-*k* dielectric gate stacks [2,4]. However, in recent years excellent device performance was shown by improving the passivation properties of high-*k*/Ge interfaces [4–6]. This was either achieved by the formation of ultrathin interfacial layers of Si/SiO_2 on top of the Ge p-channel, resulting in improved high-*k*/channel interface quality [5] or by introducing a thin interfacial layer of GeO_2 or GeON [4,6]. Only recently work on La-based rare-earth passivation of Ge surfaces is shown to yield improved device quality. The high band gap of La_2O_3 of 5.5–6.0 eV [7,8], combined with a conduction band offset of ~2.6 eV [8] and a *k*-value of 24–30 [9] make it a promising candidate to be integrated into scaled MOSFET devices. The required scaling potential of rare earth based metal–oxide–semiconductor (MOS) capacitor structures [10,11] and MOS field-effect-transistor (MOSFET) devices with equivalent oxide thickness (EOT) below 1 nm [12,13] was shown. However, in case of p-MOSFET devices still a lower mobility compared to thick GeO_2 based devices is reported. The achieved hole mobilities of 70–200 $cm^2/V\,s$ [12,14–17] are significantly lower than best reported values for thick GeO_2/Ge substrates with 575 $cm^2/V\,s$ [4]. However, as the thickness of the GeO_2 reduces the hole mobility reduces [18]. These results directly connect the improvement in Ge surface passivation with the improvement in MOSFET mobility and on-current.

In earlier works it was shown that a combination of lanthanum-oxide (La_2O_3) interfacial layers formed by Atomic Layer Deposition (ALD) capped by a thin ALD zirconium-oxide (ZrO_2) high-*k* dielectric layer can yield to a good surface passivation of the Ge surface in combination with a high overall gate dielectric constant $k \sim 21$ and EOT below 1 nm [13]. Additionally, it was shown that the presence of thin platinum (Pt) layers deposited on top of La_2O_3/ZrO_2 gate dielectric yields a decrease of the interface trap density down to the mid-10^{11} eV^{-1} cm^{-2} regime by applying an oxygen annealing step [19]. By means of XPS it was concluded that a thin oxygen

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enriched interfacial layer was formed at the ALD La_2O_3 to Ge-channel interface.

In this work we present a detailed analysis of thermal post treatments of La_2O_3/ZrO_2 gate stacks in oxidative and reductive atmosphere and give a pathway for a possible use of the processed gate dielectrics in Ge-based MOSFET devices. By doing so we are able to form a low defect density high-*k*/Ge interface in combination with the reported scalability of the presented approach.

The results suggest the formation of a $La_xGe_yO_z$ interfacial layer due to the supply of excessive oxygen during the oxidation treatment. The experiments also show that the thickness of this interfacial layer can be effectively controlled by tuning the oxygen annealing time for a given oxygen pressure and temperature. Furthermore, it is shown that an additional reduction annealing improves the electrical performance of the device structure without changing the EOT. The improvement of interfacial trap density provides a direct link of the formation of a La-based interfacial layer with excellent passivation properties with regards to the Ge interface and an enhancement of the electrical performance of MOS based device structures.

The paper is arranged as follows; in the experimental Section 2 the process flow for the formation of thin capacitor structures by deposition of La_2O_3 and ZrO_2 dielectrics by ALD on (100) Ge surfaces is discussed. The different oxidizing and reducing post deposition annealing treatments are described. In the result Section 3 the findings by capacitance–voltage (*C–V*) and conductance–frequency (*G–f*) analysis for the given oxidizing and reducing annealing treatments performed are summarized. The interface trap density is determined by the conductance method [20] from the peak of conductance divided by the frequency. In addition, these results are in conjunction with X-ray photoelectron spectroscopy (XPS), transmission electron microscopy (TEM), energy-dispersive X-ray spectroscopy (EDX) line scans and electron energy loss spectroscopy (EELS) analysis performed on the gate stacks exposed to different annealing treatments. In Section 4 possible mechanisms for the improved interface quality during the annealing treatments are discussed. Finally, the conclusion in Section 5 is correlating these results to their potential use in scaled Ge-based MOSFET devices used in future CMOS technology.

2. Experimental

2.1. Formation of gate stacks

Bulk (100) Ge *n*-type substrate with resistivity of 6–10 Ω cm were cleaned by cyclic treatment in deionized water and hydrofluoric acid (1.75%). Samples were dry blown using nitrogen and immediately transferred to the ALD reactor within 5 min. Subsequently, ALD was applied to deposit layers of 8 nm or 12 nm La_2O_3 capped by a layer of 1.5 nm ZrO_2. The Savannah 100 cross-flow reactor from Cambridge Nanotech was used. The precursors used were the La-precursor tris-(N,N′-diisopropylformamidinate)-lanthanum and the Zr-precursor tetrakis-(dimethylamino)-zirconium. Nitrogen was used as a purging gas. These precursors were kept at temperatures of 140 °C and 75 °C, respectively. As the oxygen supplying agent oxygen was used. Further information on the oxide deposition can be found in Refs. [13,19]. After the formation of the gate dielectric a thin Pt layer was deposited by sputter deposition of 5 nm Pt. From TEM images performed on cross-sections of the samples, the layer was found to be continuous. An annealing treatment in oxygen (O_2) atmosphere was performed at atmospheric pressure at temperatures of 450 °C. In earlier experiments we showed that this Pt layer will assist the oxidation process and improve the electrical properties of the later Ge–high-*k* interface [19]. A ramp rate of 10 K/s was used for the temperature adjustment. Different annealing times were used from zero seconds (s) to 3600 s. Some samples were subjected to an annealing treatment in a reducing gas atmosphere using forming gas (N_2 (90%)/H_2 (10%)) for 30 min at 350 °C. Subsequently, Pt gate electrodes with thickness of 120 nm were deposited by PVD and structured by Ar sputter etching. Circular gate contact pads with 100 μm diameter were used. Pt back contacts were sputter deposited. A schematic cross section of the final MOS structure can be found in Fig. 1.

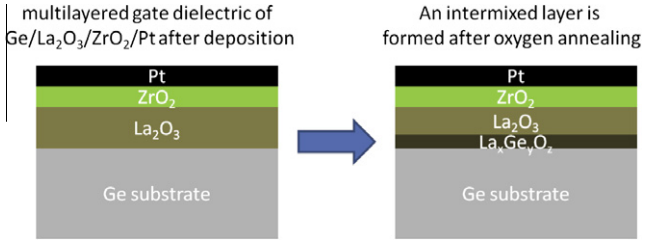

Fig. 1. Left: Schematic of ALD La_2O_3/ZrO_2 multilayered gate dielectrics with a Pt gate electrode deposited on (100) Ge wafers. Right: the gate dielectric is capped with a 5 nm thin Pt metal and is subjected to an oxidation and FGA treatment. After the oxidation treatment a thicker $La_xGe_yO_z$ interfacial layer is formed in between the Ge substrate and the La_2O_3 gate dielectric.

2.2. Electrical and structural characterization of MOS capacitor structures

For the electrical characterization, *C–V* and *G–f* measurements were performed using Keithley's semiconductor characterization system 4200. For *C–V* measurements the dc-voltage is swept from −2 V in inversion to 2 V in accumulation as well as back for measurement of hysteresis. Equivalent oxide thickness was extracted using the Hauser CVC software [21]. The oxide thickness was determined by means of a Woolams α-SE spectroscopic ellipsometry setup. XPS analysis was performed using a Specs system. Depth resolved profiles were obtained by sputter-etching the gate stack surface using Ar-ions.[1] The XPS spectra were subsequently analyzed using CasaXPS software. For investigation of Ge oxidation states the Ge 2p peak position around 1217 eV was analyzed. The procedure is further described in Ref. [19]. EELS, EDX and transmission electron microcopy (TEM) analysis were performed using a TECNAI F20, FEI setup.

3. Results

3.1. Capacitance–voltage characterization

First, the influence of the oxygen treatment on the process flow is investigated in terms of electrical properties of the gate dielectric stacks. Since it is known from earlier studies that a reaction of La_2O_3 with the Ge substrate occurs, the La_2O_3 layer thickness was intentionally selected to be relatively thick (8 nm) to allow an analysis of the structural composition of the interface region avoiding a contribution from the ZrO_2 capping layer. In a scaled MOSFET device using La_2O_3/ZrO_2 bilayer the La_2O_3 layer thickness should be decreased, as will be shown later. A gate stack consisting of 12 nm La_2O_3/1.5 nm ZrO_2 is subjected to different post deposition treatments in presence of a thin 5 nm Pt layer.

In Fig. 2a–c the influence of different annealing treatments using either O_2 annealing at 1 atm and 450 °C or N_2/H_2 annealing at 1 atm at 350 °C is compared. As a result the stretch out observed in samples of La_2O_3/ZrO_2 after only N_2/H_2-annealing treatment in

[1] Experiments evaluating the possibility of using aqua regia for removing the Pt from the dielectric surface were performed (unpublished).

the C–V curves vanishes even after very short oxygen annealing times of 20 s. From comparison of capacitance voltage characteristics obtained for longer oxygen annealing times a negative shift of flatband voltage is observed. Starting from the case of no oxygen annealing the flatband voltage is shifted to more negative values after a short anneal in oxygen for 20 s whereat a flatband voltage amounts to +0.24 V is measured. This value is further shifted to a negative value of −0.15 V after the oxidation treatment for 3600 s. A reduced humping near flatband voltage displays the decrease of the density of electrical active interface traps (D_{it}) near the Ge midgap. The gate voltage corresponding to the midgap position is obtained by fitting the respective CV curve to an ideal CV curve using the Hauser software [21]. Furthermore, a reduced hysteresis of ∼100 mV is found after the oxygen annealing treatment. However, for longer annealing times a reduced oxide capacitance is found.

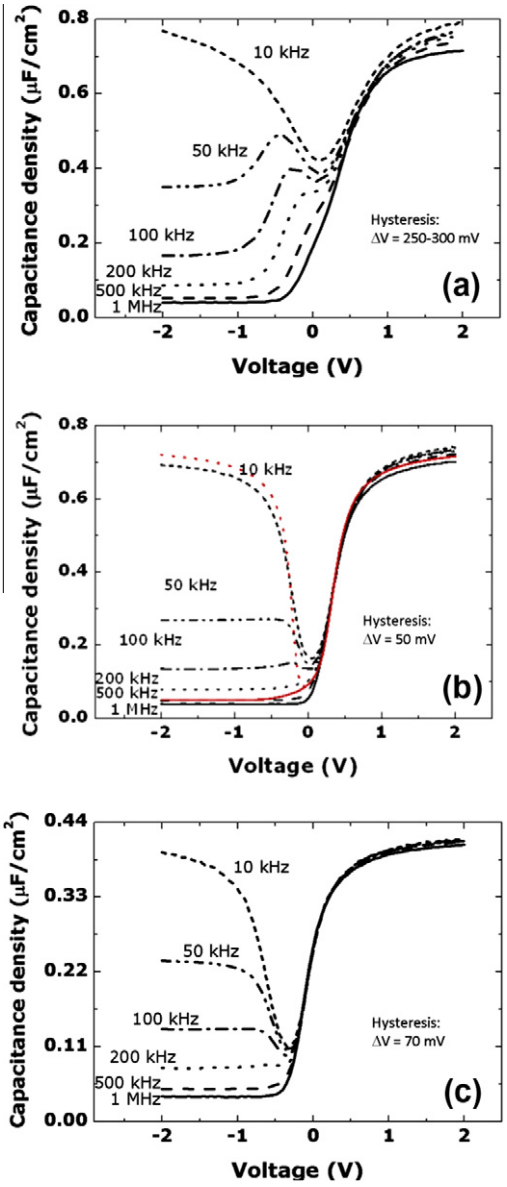

Fig. 2. C–V characteristics of 12 nm La_2O_3 capped with 1.5 nm ZrO_2 deposited by ALD on (100) n-type Ge substrates. Before the post deposition annealing treatment a thin layer of 5 nm Pt is deposited by sputter deposition. (a) A reduction annealing in N_2/H_2 atmosphere at 350 °C for 30 min is applied; (b) an oxidation treatment at 1 atm at 450 °C for 20 s is applied before the FGA at 350 °C for 30 min; or; (c) an oxidation treatment at 1 atm at 450 °C for 3600 s is applied before the FGA at 350 °C for 30 min. After the different annealing treatments Pt gate electrodes are deposited and structured by sputter etching. The bump in (a) at ∼−0.7 V is related to weak inversion response as pointed out in Ref. [31]. Note that the scale for graph (c) is different from graph (a) and (b). Simulated capacitance voltage characteristics for low (red, drawn line) and high (red, dotted line) measurement frequencies are additionally shown in (b). The curves are obtained by using Hauser CVC software [21] and fitting to experimental data for measurement frequencies of 500 kHz.

3.2. Interface trap density and equivalent oxide thickness

To further analyze the trade-off between the reduced D_{it} and the increased EOT of the presented layer structure of Ge/12 nm La_2O_3/1.5 nm ZrO_2, different oxide annealing times were applied starting from zero seconds up to 3600 s. The results of D_{it} for the different oxidizing and reducing annealing treatments are reported in Fig. 3. It can be clearly seen that the interface trap density is lowered with longer oxygen annealing times. The respective conductance frequency measurements are reported in Fig. 4 for the three shortest oxygen annealing times. Interestingly, this positive effect is even improved by performing the subsequent N_2/H_2 annealing treatment at 350 °C for 30 min in addition to the oxidizing annealing treatment. Here, an interface trap density down to $\sim 3 \times 10^{11}\,eV^{-1}\,cm^{-2}$ can be achieved. In addition, only little change in the EOT is found after the respective N_2/H_2 treatment

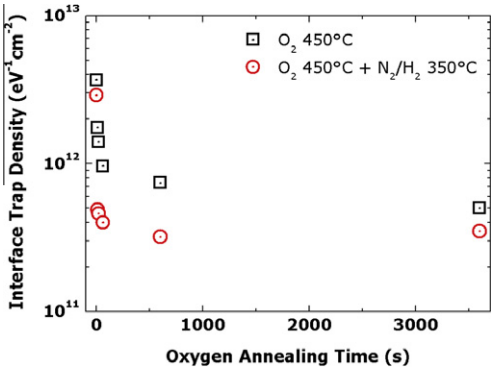

Fig. 3. Interface trap density near mid-gap obtained from G–f measurements for a layer structure of 12 nm La_2O_3/1.5 nm ZrO_2. Different oxygen annealing treatments are applied in presence of a 5 nm thin Pt capping layer at a O_2 pressure of 1 atm. An additional treatment in N_2/H_2 atmosphere for 30 min at 350 °C improves the interface trap density to a low value of $\sim 3 \times 10^{11}\,eV^{-1}\,cm^{-2}$.

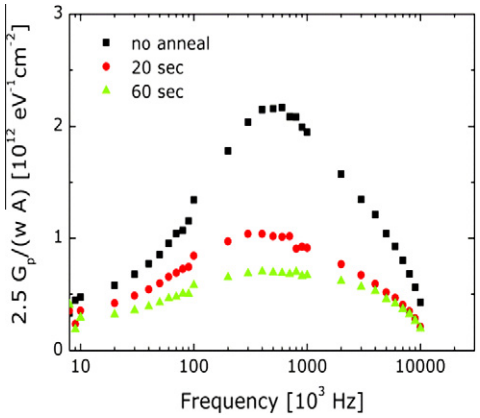

Fig. 4. Typical conductance measurements are shown as a function of frequency for the layer structure of 12 nm La_2O_3/1.5 nm ZrO_2. The result for samples subjected to no oxygen anneal, a 20 s and a 60 s oxygen anneal are compared. The respective interface trap density was obtained from the peak of the measured conductance divided by the capacitor area and measurement frequency according to the conductance method [20].

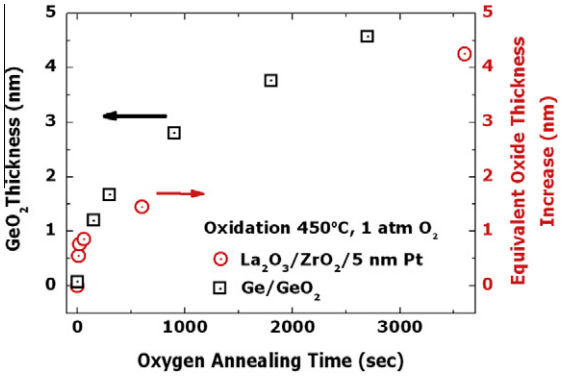

Fig. 5. Increase in EOT as a function of oxygen annealing time at 1 atm at 450 °C for a layer of 12 nm La_2O_3/1.5 nm ZrO_2. The starting value of EOT is 3.8 nm. Nearly no change in the measured EOT after performing an additional reduction annealing step in N_2/H_2 is observed (not shown). Additionally, the oxidation of a clean Ge surface is shown. Here, the physical GeO_2 oxide thickness is shown. The surface is subjected to the same oxidation treatment at 450 °C at 1 atm.

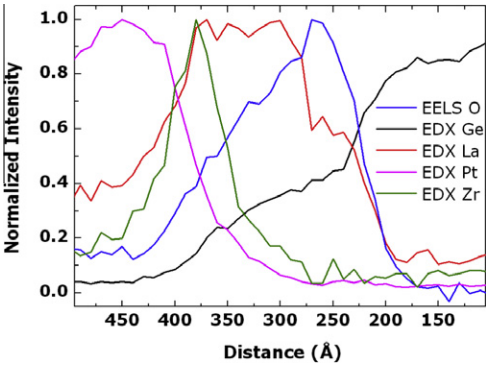

Fig. 7. EELS and EDX line scan analysis of 12 nm La_2O_3/1.5 nm ZrO_2 after oxygen annealing treatment for 3600 s at 1 atm and 450 °C. An intermixed interfacial layer of Ge, La and O is observed at the La_2O_3/Ge interface.

(not shown) compared to samples not subjected to the FGA treatment after oxidation. In Fig. 5 the dependence of the measured equivalent oxide thickness during thermal oxidation treatment at 450 °C at 1 atm O_2 is shown. Starting with an EOT of 3.8 nm for the layer structure of 12 nm La_2O_3/1.5 nm ZrO_2 increased EOT's are found in the first 10–60 s of the oxygen annealing treatment from 0.5 to 0.8 nm. As a comparison the formation of GeO_2 on bare Ge substrates from thermal oxidation grown performed at atmospheric pressure at 450° is shown. A similar growth characteristic is found.

3.3. Structural characterization

In order to investigate the structural properties of the gate dielectric to Ge interface different analysis methods were applied. TEM analysis was performed on stacks of 12 nm La_2O_3/1.5 nm ZrO_2 which were annealed for either 60 s or 3600 s in oxygen at 450 °C. Fig. 6 shows the respective results for the gate stacks exposed to the oxygen annealing treatment in presence of the thin Pt layer. Comparing the two gate stacks an increase in the interfacial layer thickness can be observed in case of the longer annealing time. The lighter contrast of this interlayer in TEM images also suggests the enrichment in lighter elements that would be expected in case of increased oxygen incorporation. This is also consistent with an oxygen densification in the interlayer as pointed out by Tsoutsou and coworkers [22]. From the combination of TEM analysis and CV measurements of the samples oxidized for either 60 s or 3600 s the dielectric constant of the interfacial layer can be extracted with $k = 8–9$. This is in good agreement with the reported value for $La_xGe_yO_z$ of 9–11 [23]. Assuming a change of 0.5 nm in EOT for oxygen annealing times for the case of 10 s O_2 annealing (as found from Fig. 5) an additional formation of a 1.1 nm $La_xGe_yO_z$ interfacial layer can be assumed. Interestingly, a strong surface roughening is present for long oxygen annealing times as can be seen from the interface of $La_xGe_yO_z$ with Ge.

To analyze in more detail the formation of the interfacial layer at the La_2O_3 to Ge interface a further compositional analysis is performed on the shown TEM cross-sections. Fig. 7 shows the results of depth resolved EELS analysis for the O profile in combination with EDX line scans for Ge, La, Pt and Zr performed at samples with 12 nm La_2O_3/1.5 nm ZrO_2 on Ge. These samples were also subjected to a 3600 s annealing in O_2 at 450 °C. As can be seen from the La and Ge peaks, at the interface between La_2O_3 and Ge an intermixed layer is formed. The data of the Ge signal indicates a Ge or GeO [24] in-diffusion into the La_2O_3 dielectric layer. These results are further supported by results from depth resolved XPS analysis applied for a stack of 8 nm La_2O_3/1.5 nm ZrO_2 subjected to the same oxygen annealing treatment seen in Fig. 8. Here the line spectra for La 3d 5/2 was recorded in a range of 830–844 eV, O 1s in a range of 525–535 eV, Zr 3d in a range of 174–188 and Pt 4f in a range of 64–80 eV. Fig. 9 is additionally showing the narrow scan for these XPS analysis around the Ge 2p peak energy for different sputter times of the gate dielectric stack. The peak was re-

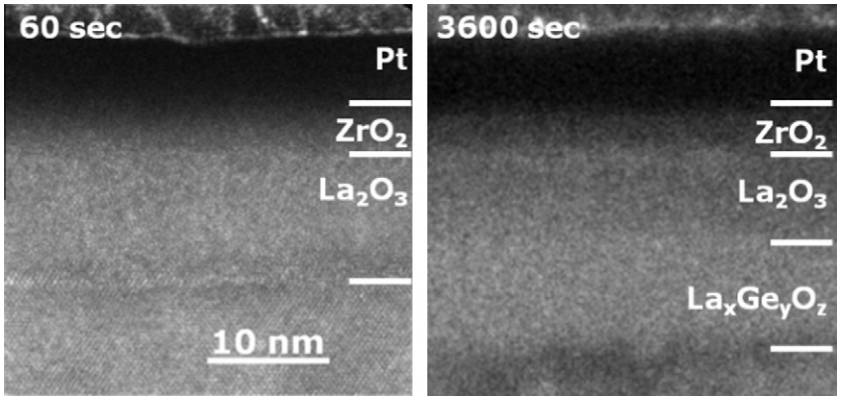

Fig. 6. TEM analysis of 12 nm La_2O_3/1.5 nm ZrO_2 annealed for 60 s (left) or 3600 s (right) on O_2 1 atm at 450 °C in presence of 5 nm Pt capping layer. Three distinct layers on top of the Ge substrate can be identified, which are La_2O_3, a thin ZrO_2, and the thin Pt capping layer structure (dark contrast). In addition, the formation of a lighter contrast interfacial layer can be seen for long oxygen annealing treatment of 3600 s (right).

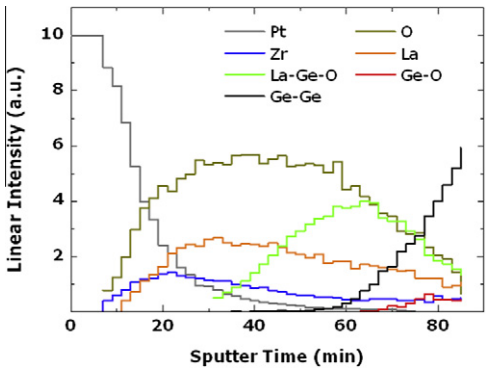

Fig. 8. Depth resolved XPS analysis applied to a layer structure of 8 nm La_2O_3/1.5 nm ZrO_2 subjected to an oxygen annealing treatment of 3600 s at 450 °C and 1 atm. A clear signal of La–Ge–O signal can be found at the interface of Ge–La_2O_3 interface. Here, La–Ge–O denotes the Ge binding state shifted by 2.3 eV with respect to the Ge 2p peak position (Ge–Ge) and Ge–O the Ge^{2+} oxidation state shifted by 1.5 eV.

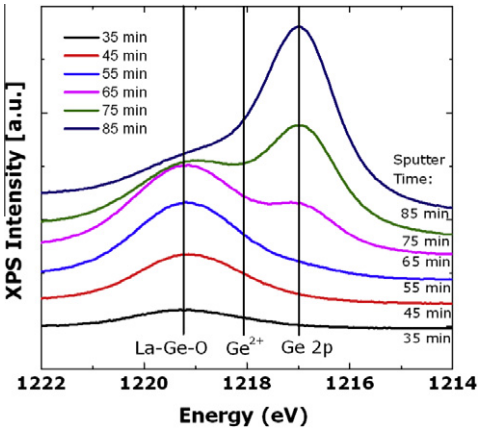

Fig. 9. Narrow spectrum of Ge 2p XPS signal around Ge 2p peak position. The intensity of curves is shifted by a constant offset for the different sputter times shown.

corded from 1214 to 1222 eV. As can be seen first a peak shifted by ~2.3 eV is observed, related to La–Ge–O bonding [25]. Finally, the Ge 2p signal is obtained related to the Ge substrate. This is in well agreement with a formation of a $La_xGe_yO_z$ interfacial layer.

4. Discussion

In order to understand the improvement in measured electrical characteristics with the respective annealing treatment, first, the formation of the $La_xGe_yO_z$ interfacial layer shall be discussed. After the wet chemical processing for cleaning of the Ge substrates samples are subjected to cleanroom atmosphere and transferred to the ALD reaction chamber within several minutes. However, it is expected that a thin GeO_x suboxide forms in this processing scheme. It was pointed out by Houssa and coworkers that La_2O_3 in contact to the GeO_x results in the formation of only La–O–Ge bonds near the interface. The reason is the fourfold coordination of La atoms in the GeO_x matrix. Interestingly, the resulting band structure of Ge at the interface is free of surface states and thus, La_2O_3 layers are predicted to show a good passivation of the Ge surface [23]. Further on, the samples are subjected to an oxide annealing treatment. Here, the driving force for the formation of $La_xGe_yO_z$ interfacial layers is suggested to be related to oxide densification as proposed by Tsoutsou and coworkers [22]. This theory proposes that the less dense oxide La_2O_3 with its strong electropositive La atom tries to attract as much oxygen atoms to its surrounding as possible, thereby reacting with the more oxygen dense GeO_2 species [11]. The constant increased supply of oxygen during the oxygen annealing is thus leading to the observed growth of a thick $La_xGe_yO_z$ interlayer, instead of a formation of interfacial GeO_2. This is in agreement with the finding of an interfacial layer with a value of $k = 8–9$ which was obtained by comparison of TEM and $C–V$ analysis. As we report in [19] a thin Pt cap layer deposited before the oxidation annealing further assists the oxidation process, most likely by the formation of atomic oxygen by dissociating O_2 molecules from the oxygen gas atmosphere.

No change in the equivalent oxide thickness is observed during the forming gas anneal. This suggests that hydrogen species leave the $La_xGe_yO_z$ layer thickness constant without any further layer growth. As a result lowest interface trap densities down to $3 \times 10^{11}\ eV^{-1}\ cm^{-2}$ are achieved. Remarkably, in the case where the gate stacks are not subjected to an oxidation anneal before the FGA, little or no improvement of the interface trap density is observed, as can be seen from Fig. 3. This refers to the first data point, of 0 s oxygen anneal. For these samples we assume that no or only a thin $La_xGe_yO_z$ interfacial layer is present. A similar improvement in interface trap density was observed for MBE La_2O_3 layers in contact to (100)-Ge after forming a La – germinate interfacial layer [15]. Our results for ALD La_2O_3/ZrO_2 are similar to results reported for ALD grown Al_2O_3 on interfacial GeO_2 with D_{it} of low to mid-$10^{11}\ eV^{-1}\ cm^{-2}$ [26], high-pressure oxidized Ge-(111)/Y_2O_3 of $\sim 10^{11}\ eV^{-1}\ cm^{-2}$ [27] and are well below reported values for Ge in direct contact to ZrO_2 or HfO_2 with $>10^{12}\ eV^{-1}\ cm^{-2}$ [2].

Several studies address the passivation properties of high-k dielectrics in contact to Ge surfaces [28]. In general two types of concerns are addressed. These are either the diffusion of volatilization byproducts from annealing of Ge substrates such as Ge or GeO atoms [11,29] or the intrinsic defects related to the defective Ge surface [11,23]. It is known that by forming a $La_xGe_yO_z$ interlayer the formation of volatile GeO species is suppressed. Furthermore, as was found by combination of XPS and UPS, a $La_xGe_yO_z$ interlayer might improve the intrinsic defects present at the Ge surface, which are responsible for Fermi-Level pinning [11]. Since we observe the strongest improvement in interface trap densities already within short oxygen annealing times and thus, during the formation of a thin $La_xGe_yO_z$ interfacial layer in contact with Ge, the improved electrical passivation can be related to the $La_xGe_yO_z$ layer. The observed negative shift in flatband voltage could additionally be related to a lowered amount of interface charge density D_{it} during the oxygen anneal as discussed by Tsipas and Dimoulas [23]. However, this shift of threshold voltage might also be caused by an increased number of fixed charges. Addressing the performance of MOSFET devices, it is not clear if this improvement of interface trap density can be translated to improved device characteristics. No improved mobility in gate stacks of Al_2O_3/La_2O_3/Ge was observed by Rossel and coworkers [16]. However, other reports by Andersson and coworkers suggest a positive influence of FGA in both D_{it} and mobility of holes in p-channel devices using comparable gate dielectric stacks of HfO_2/La_2O_3/Ge [15].

For the presented oxygen annealing approach equivalent oxide thicknesses of 1.2–1.43 nm can be achieved in case of a 1 nm thin La_2O_3 interfacial layer capped by a thicker layer of 7 nm ZrO_2 as reported in Ref. [19]. We note that for such thin layers of La_2O_3 a $La_xGe_yO_z$ interlayer can be already observed after deposition of ZrO_2 by ALD [30]. In general, the thickness of the $La_xGe_yO_z$ interfacial layer with a lower k-value of 8–9 as shown in this study, should be optimized in order to find a good passivation of surface defects while keeping the equivalent oxide thickness low. Concerning this issue, our results suggest that a thin $La_xGe_yO_z$ interlayer with thickness of ~1.1 nm already formed after 10 s oxygen annealing pro-

vides a good surface passivation with density of interface states in the low 10^{11} eV^{-1} cm^{-2} range and a related additional trade-off in EOT of only 0.5 nm.

5. Conclusion

A pathway for improving the interface quality of ALD deposited La_2O_3 interface passivation layers on Ge substrates is given. These layers were capped with ZrO_2 and furthermore a Pt-assisted oxidation process in combination with a reduction annealing treatment in N_2/H_2 was applied. For a layered gate stack structure of Ge/La_2O_3/ZrO_2/Pt it was shown that interface trap densities down to $\sim 3 \times 10^{11}$ eV^{-1} cm^{-2} can be achieved in combination with minimal discount in EOT of 0.5 nm for short time annealing in oxygen atmosphere and a subsequent annealing step in reducing atmosphere. As the main driving force of this improvement the formation of a La–germanate interfacial layer was identified with dielectric constant of 8–9. An improved surface passivation was achieved already for thin $La_xGe_yO_z$ interfacial layers with thickness of 1–2 nm and minimal EOT offset. Thus a trade-off between improved surface quality and scalability of the presented approach was observed. However, the interlayer thickness was found to be adjustable by the time of an oxide annealing treatment. In a similar way the interlayer thickness may be adjustable by choosing a La_2O_3 starting thickness smaller than the value of 8 or 12 nm reported in this study. In summary, the presented results give evidence for an efficient approach to improve the electrical surface passivation required for future Ge-based MOSFET device technology. Additionally, the insertion of the thin Pt metal interlayer with a high vacuum work function may also offer advantages in Ge-pMOSFET device performance.

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